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(11)

EP 1 357 611 A1

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**EUROPEAN PATENT APPLICATION**

published in accordance with Art. 158(3) EPC

(43) Date of publication:

29.10.2003 Bulletin 2003/44

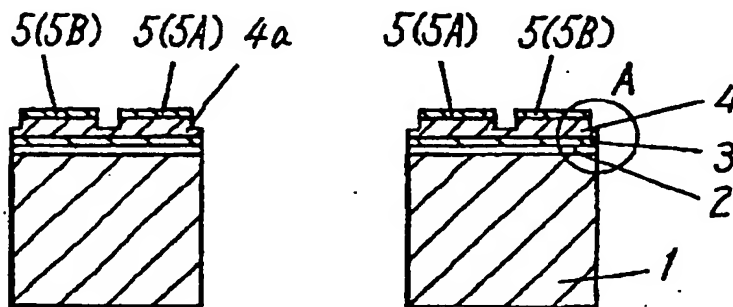
(51) Int Cl.7: **H01L 41/09**, H01L 41/24,  
G01P 9/04, G01C 19/56(21) Application number: **02760562.5**(86) International application number:  
**PCT/JP02/08056**(22) Date of filing: **07.08.2002**(87) International publication number:  
**WO 03/019690 (06.03.2003 Gazette 2003/10)**

(84) Designated Contracting States:

**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR  
IE IT LI LU MC NL PT SE TR**(72) Inventor: **NAKATANI, Masaya****Takarazuka-shi, Hyogo 665-0054 (JP)**(30) Priority: **27.08.2001 JP 2001255689****15.10.2001 JP 2001316431**(74) Representative: **Schuster, Thomas, Dipl.-Phys.****Grünecker, Kinkeldey, Stockmair &****Schwanhäusser****Anwaltssozietät****Maximilianstrasse 58****80538 München (DE)**(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL  
CO., LTD.****Kadoma-shi, Osaka 571-8501 (JP)****(54) PIEZOELECTRIC FUNCTIONAL PART AND METHOD OF MANUFACTURING THE PART**

(57) A piezoelectric device includes a substrate, a buffer layer on the substrate, a lower electrode layer on the buffer layer, a piezoelectric layer on the lower electrode layer, and an upper electrode layer on the piezoelectric layer. The piezoelectric layer has a base portion

extending outwardly at its lower portion of its periphery. The piezoelectric device provides enhanced bonding strength between the substrate and the stacked structure including the upper electrode layer, the lower electrode layer, and the piezoelectric layer.

**FIG. 14**

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FP 03-0299
-00 EP-TD
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SEARCH REPORT

## Description

### TECHNICAL FIELD

[0001] The present invention relates to piezoelectric devices, such as a sensor, an actuator, memory, and an optical switch, and to a method of manufacturing the device.

### BACKGROUND ART

[0002] A conventional piezoelectric device includes a substrate, a lower electrode layer on a surface of the substrate, a piezoelectric layer, and an upper electrode layer which are stacked in this order. When a voltage is applied to the upper electrode layer, the piezoelectric layer deforms due to an electric field developed between the upper and lower layers, thereby providing the device with a variety of functions.

[0003] In the conventional piezoelectric device, however, a stacked structure including the upper and lower electrode layers and the piezoelectric layer has poor strength in bonding with the substrate. Applying the voltage to the upper and lower layers deforms the piezoelectric layer, and this causes stress to the substrate. In the conventional piezoelectric device, the upper and lower electrode layers and the piezoelectric layer, being sized substantially the same, are bonded with the substrate. The poor bonding between the lower electrode layer and the substrate causes them to be peeled off.

### DISCLOSURE OF THE INVENTION

[0004] A piezoelectric device includes a substrate, a lower electrode layer over the substrate, a piezoelectric layer disposed on the lower electrode layer and having a base portion outwardly extending at a portion toward the lower electrode layer, an upper electrode layer on the piezoelectric layer. The base portion is formed at a lower portion of a peripheral face of the piezoelectric layer and extends outwardly from the peripheral face. The piezoelectric layer and the lower electrode layer have areas larger than an area of the upper electrode layer, enhancing strength in bonding. The extending base portion lengthens a creeping distance between the upper and lower electrode layers, thus protecting the electrode layers from being short circuited between the electrode layers.

### BRIEF DESCRIPTION OF THE DRAWINGS

#### [0005]

Fig. 1 is a perspective view of an angular velocity sensor according to an exemplary embodiment of the present invention.

Fig. 2 is an exploded perspective view of the angular velocity sensor according to the embodiment.

Fig. 3 is a flow chart of a process for manufacturing the angular velocity sensor according to the embodiment.

Fig. 4 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 5 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 6 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 7 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 8 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 9 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 10 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 11 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 12 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 13 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 14 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 15 is a sectional view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 16 is a perspective view of the angular velocity sensor for showing the process according to the embodiment.

Fig. 17 is a perspective view of the angular velocity sensor for showing the process according to the embodiment.

### DESCRIPTION OF THE PREFERRED EMBODIMENT

[0006] Fig. 1 shows an angular velocity sensor as a piezoelectric device of an exemplary embodiment of the present invention. As shown in an exploded perspective view of Fig. 2, the angular velocity sensor includes a tuning-fork-shaped substrate 1 made of silicon, and further includes a buffer layer 2; a lower electrode layer 3; a piezoelectric layer 4; and an upper electrode layer 5, which are stacked on the substrate in this order.

[0007] An operation of the angular velocity sensor for detecting an angular velocity will be described with ref-

erence to Fig. 1. The upper electrode layer 5 includes an exciting electrode 5A and a detecting electrode 5B, which are disposed opposite to the lower electrode layer 3 as to sandwich the piezoelectric layer 4 with the layer 3. A voltage applied to an area between the exciting electrode 5A and the lower electrode layer 3 expands and contracts the piezoelectric layer 4 sandwiched between the layers 5A and 3, thereby deforming two arms 10A and 10B of the tuning-fork-shaped substrate 1. The arms 10A and 10B vibrate laterally against the tuning-fork shape. When an angular velocity having its axis parallel to the arms 10A and 10B is applied, the arms have a warp in the direction perpendicular to the axis of the angular velocity and a vibrating direction of the arms. The amount of the warp is detected by the detecting electrode 5B. In the angular velocity sensor, excitation for the arms 10A and 10B and the amount of the angular velocity are detected through the piezoelectric layer 4.

[0008] The angular velocity sensor will be described in detail with reference to Fig. 2. The angular velocity sensor includes the tuning-fork-shaped substrate 1 made of silicon, the buffer layer 2 on the substrate, and the lower electrode layer 3 on the layer 2. Each of the layers 2 and 3 has a shape substantially identical to that of the substrate 1. The sensor further includes the piezoelectric layer 4 on the lower electrode layer 3 and the upper electrode layer 5 on the piezoelectric layer 4. The piezoelectric layer 4 has its upper portion having a shape identical to that of the upper electrode layer 5 and its lower portion having a shape identical to that of the lower electrode layer 3, as shown in Fig. 2. The lower portion of the piezoelectric layer 4 has a larger area outwardly extending as a base portion (which will be described later). The lower electrode layer 3 beneath the piezoelectric layer 4 has a substantial area since having the same shape as the layer 4 having the base portion, thus being bonded on the substrate 1 the buffer layer 2 securely. Therefore, even if the piezoelectric layer 4 expands and contracts by applying the voltage between the upper layer 5 and the lower layer 3, its stacked structure is hardly peeled off from the substrate 1. Furthermore, the extended base portion lengthens a creeping distance between the upper layer 5 and the lower electrode layer 3, thus protecting the electrode layers from being short circuited between the layers.

[0009] The buffer layer 2 of the angular velocity sensor is made of one of NiO, CoO, MgO, and Ti. The lower electrode layer 3 is made of Pt. The piezoelectric layer 4 is made of lead titanate zirconate. The upper electrode layer is made of Au. The piezoelectric layer 4 is thicker than the buffer layer 2, the lower electrode layer 3, and the upper electrode layer 5. The thickness allows the piezoelectric layer 4 to have the outwardly extending base portion formed easily. The base portion lengthens the creeping distance between the upper and lower layers 5 and 3, thus protecting the electrode layers 5 and 3 from short-circuit between the electrode layers.

[0010] An auxiliary electrode 6 shown in Figs. 1 and

2 is formed to lead the lower electrode layer 3 to a surface.

[0011] A method of manufacturing the angular velocity sensor will be described with reference to accompanying drawings. Although plural angular velocity sensors are simultaneously formed on a substrate in a manufacturing process, an explanation is given to one of them. Fig. 3 illustrates the process of manufacturing the angular velocity sensor according to the embodiment. A procedure of the manufacturing will be explained with reference to Figs. 4 through 15.

[0012] First, the buffer layer 2 of NiO is formed on a surface of a silicon-made substrate 1, as shown in Fig. 4, so that NiO has a crystal orientation of (1, 0, 0) (STEP 1 of Fig. 3). The buffer layer 2 is formed by metal organic chemical vapor deposition (MOCVD) employing gas, such as sublimated and vaporized nickel acetylacetonate. Next, the lower electrode layer 3 is formed by sputtering Pt, as shown in Fig. 5 (STEP 2 of Fig. 3). Then, as shown in Fig. 6, the piezoelectric layer 4 is formed by sputtering lead titanate zirconate (STEP 3 of Fig. 3). Then, in Fig. 7, the upper electrode layer 5 is formed by sputtering or vacuum evaporation of Au (STEP 4 of Fig. 3).

[0013] For forming the gold (Au) layer is formed, thin chromium (Cr)-layer or titanium (Ti)-layer preferably formed on the substrate before the Au-layer is provided. The layers allow the Au-layer to have higher strength in bonding. According to an experiment by the inventor, the Ti-layer having a thickness ranging from about 20 to 100 Å on the substrate by vacuum evaporation provides sufficient adhesion. In conventional piezoelectric devices, it has been difficult to form a piezoelectric layer 4 exhibiting high piezoelectric characteristics on a silicon-made substrate 1. However, the buffer layer 2 described above allows the piezoelectric layer 4 to be made of lead titanate zirconate, thereby providing excellent piezoelectric characteristics.

[0014] Figs. 8 through 15 shows sectional views of the arms 10A and 10B of tuning-fork-shaped portion in Fig. 1. Throughout the drawings, the left side of a drawing corresponds to the arm 10A of Fig. 1, while the right side corresponds to the arm 10B of Fig. 1.

[0015] Following to STEP 4 of Fig. 3, as shown in Fig. 8, a first resist film 7 is formed on the upper electrode layer 5 (STEP 5 of Fig. 3). Then, in Fig. 9, the electrode layer 5 and the piezoelectric layer 4 are etched by dry etching (STEP 6 of Fig. 3). In this process, the etching is stopped in the piezoelectric layer 4 before the etching is performed to the lower electrode layer 3. Next, as shown in Fig. 10, the first resist film 7 is peeled off from the upper electrode layer 5 (STEP 7 of Fig. 3), and thereby, the upper electrode layer 5 is separated into the exciting electrode 5A and the detecting electrode 5B. Then, as shown in Fig. 11, a second resist film 8 is formed on the upper electrode layer 5. A periphery of the film 8 covers the etched edge of the upper electrode layer 5 and an etched side face a small portion of the

etched surface of the piezoelectric layer 4 (STEP 8 of Fig. 3). Next, as shown in Fig. 12, the piezoelectric layer 4, the lower electrode layer 3, and the buffer layer 2 are etched away so that the substrate 1 is exposed (STEP 9 of Fig. 3).

[0016] The process above allows the piezoelectric layer 4 to have the base portion 4a extending outwardly at its lower portion of the periphery, as shown in section A of Fig. 14. The piezoelectric layer 4 having the base portion securely contacts the lower electrode layer 3 through a sufficient area. According to an experiment by the inventor, the piezoelectric layer 4 having no base portion was easily stripped off, while the layer 4 having the base portion was hardly stripped off.

[0017] Following STEP 9, the silicon-made substrate 1 is etched by dry etching (STEP 10 of Fig. 3). In the etching process above, the substrate 1 is etched by etching gas different from that used for the piezoelectric layer 4, the lower electrode layer 3, and buffer layer 2 in Fig. 12. The same gas undesirably etches the layers 2, 3, and 4 due to intrusion of the gas from their sides. For example, gas containing  $CF_4$  and Ar is used for the layers 2, 3, and 4, and gas containing  $SF_6$ ,  $O_2$ , and  $C_4F_8$  is used for the substrate 1. This enables the substrate 1 to be etched in the vertical downward direction in Fig. 13 with no harm to the base portion 4a of the piezoelectric layer 4, after the layers 2, 3, and 4 are etched away.

[0018] In the final process shown in Fig. 14, the second resist film 8 is removed by oxygen-ashing or other methods (STEP 11 of Fig. 3). As described above, the angular velocity sensor shown in Fig. 1, in which the piezoelectric layer 4 has the base portion 4A extending outwardly at its lower side of the periphery, is provided.

[0019] In the method described above, the silicon substrate 1 is dry-etched in a vertical downward direction, since the portion of the substrate 1 beneath the base portion 4a formed at the lower portion of the piezoelectric layer 4 is not etched. Under the consideration that the upper layer 5, the lower layer 3, and the piezoelectric layer 4 are stacked over only one surface of the substrate 1, it may be necessary to decrease the mass of the other surface of the substrate 1 to bring the substrate 1 into balance.

[0020] In this case, the substrate 1 may be etched so as to slender toward its bottom, as shown in Fig. 15, with etching gas containing  $SF_6$  and  $O_2$  increased and  $C_4F_8$  decreased. The gas allows the substrate 1 to have strongly-etched surface opposite to the surface having the buffer layer 2 thereon, thus tapering off the substrate 1 toward its bottom, as shown in Fig. 15.

[0021] As mentioned above, the single angular velocity sensor is described. The case in which plural sensors are simultaneously formed will be described.

[0022] Fig. 16 illustrates a dry-etching process of a silicon substrate 13. The substrate 13 to be etched is bonded to a glass-made dummy substrate 14 through a bonding member 15. The bonding member 15 is formed of material having a color different than the silicon sub-

strate 13, for example, paste containing white alumina particles. Removing an unnecessary surface of the substrate 13 by dry-etching exposes the colored bonding member 15, which shows completion of etching at a glance. After the silicon substrate 13 is etched, angular velocity sensors 16 are separated into individual pieces. Before the separation, the dummy substrate 14 securely holds the individual pieces of the angular velocity sensors 16 through the bonding member 15 so as not to allow the sensors to come apart. Another advantage is that the dummy substrate 14 made of glass has an exposed surface unaffected by the etching gas while the substrate 13 is being etched or after the substrate 13 is etched, thereby providing etching with high consistency. In the process, a resist film 12 is disposed on the substrate 13.

[0023] According to the embodiment, the buffer layer 2 allows the piezoelectric layer 4 to be securely bonded to the silicon substrate 1 via the lower electrode layer 3. The lower electrode 3 may be formed of platinum (Pt) containing 1 to 15% of titanium (Ti), and thus, the mixed Ti is aligned in a manner identical to a lattice constant of the piezoelectric layer 4 on the Pt-layer. The lower electrode layer 3 can securely hold the buffer layer 2 without the buffer layer 2. An angular velocity sensor which does not have the buffer layer 2 is manufactured by the method above, in which the process of forming the buffer layer 2 is simply omitted from the procedure.

[0024] An angular velocity sensor is described as just an example of piezoelectric devices according to the embodiment, but it is not limited to the sensor. The present invention can be applicable to any piezoelectric devices including a piezoelectric body, such as a sensor, an actuator, a memory, and an optical switch, as long as the device has electrodes and a piezoelectric layer 4 sandwiched between the layers, and as long as the device utilizes a change in characteristics, e.g. a warp, and a change in permittivity, of the piezoelectric layer 4 caused by a of voltage applied to the electrodes.

#### INDUSTRIAL APPLICABILITY

[0025] A piezoelectric device of the present invention, as described above, includes a piezoelectric layer having an outwardly extending base portion formed at its lower of its periphery. This arrangement allows the piezoelectric layer, a lower electrode layer, and a buffer layer underlying have areas larger than the area of an upper electrode layer. The layers contact a substrate through the large area, thus having an enhanced strength in bonding. The base portion lengthens a creeping distance between the upper and lower electrode layers, thus protecting the electrode layers from short-circuiting between the electrode layers.

## Claims

1. A piezoelectric device comprising:
  - a substrate;
  - a lower electrode layer disposed over said substrate;
  - a piezoelectric layer disposed on the lower electrode layer, said piezoelectric layer including a base portion extending outwardly on said lower electrode layer;
  - an upper electrode layer disposed on said piezoelectric layer.
2. The piezoelectric device of claim 1, wherein said substrate has a tuning-fork shape.
3. The piezoelectric device of claim 1, further includes a buffer layer disposed on said substrate.
4. The piezoelectric device of claim 3, wherein said buffer layer contains at least one of NiO, CoO, MgO, and Ti, said lower electrode layer contains Pt, said piezoelectric layer contains lead titanate zirconate, and said upper electrode layer contains Au.
5. The piezoelectric device of claim 2, wherein said piezoelectric layer is thicker than said buffer layer, said upper electrode layer, and said lower electrode layer.
6. The piezoelectric device of claim 1, wherein said lower electrode layer is formed of Pt including 1 to 15% of Ti mixed therein, said piezoelectric layer contains lead titanate zirconate, and said upper electrode layer contains Au.
7. The piezoelectric device of claim 6, wherein said piezoelectric layer is thicker than said buffer layer, said upper electrode layer, and said lower electrode layer.
8. A method of manufacturing a piezoelectric device, comprising the steps of:
  - stacking a buffer layer on a substrate, a lower electrode layer on the buffer layer, a piezoelectric layer on the lower electrode layer, and an upper electrode layer on the piezoelectric layer;
  - forming a first resist film on the upper electrode layer;
  - etching a portion of the piezoelectric layer uncovered with the first resist film exclusive of a lower portion of the piezoelectric layer toward the lower electrode;
  - stripping off the first resist film;
  - forming a second resist film on the upper electrode layer covered with the first resist film and
- on a surface of the lower portion of the piezoelectric layer; and
- etching portions of the buffer layer, the lower electrode layer, and the piezoelectric layer to expose a surface of the substrate, the portions being uncovered with the second resist film.
9. The method of claim 8, wherein the buffer layer contains at least one of NiO, CoO, MgO, and Ti, the lower electrode layer contains Pt, the piezoelectric layer contains lead titanate zirconate, and the upper electrode layer contains Au.
10. The method of claim 8,
  - wherein the substrate contains Si, and
  - wherein said step of etching portions of the buffer layer, the lower electrode layer, and the piezoelectric layer uncovered with the second resist film comprises the sub-steps of:
    - etching the buffer layer, the lower electrode layer, and the piezoelectric layer by first etching gas; and
    - then, etching the buffer layer, the lower electrode layer, and the piezoelectric layer by second etching gas.
11. The method of claim 10, further comprising the step of:
  - etching the substrate so as to increase an etched portion thereof toward a surface thereof opposite to a surface thereof on which the buffer layer is disposed.
12. The method of claim 10, wherein said step of etching the substrate comprises the sub-step of etching the substrate having a dummy substrate bonded thereto, with a bonding member, on the surface thereof on which the buffer layer is disposed surface.
13. The method of claim 12, wherein the dummy substrate is made of glass, and the bonding member has a color different from a color of the substrate.
14. A method of manufacturing a piezoelectric device, comprising the steps of:
  - stacking a lower electrode layer on a substrate, a piezoelectric layer on the lower electrode layer, and an upper electrode layer on the piezoelectric layer;
  - forming a first resist film on the upper electrode layer;
  - etching a portion of the piezoelectric layer uncovered with the first resist film exclusive of a lower portion of the piezoelectric layer toward

the lower electrode;  
stripping off the first resist film;  
forming a second resist film on the upper electrode layer covered with the first resist film and a surface of the lower portion of the piezoelectric layer; and  
etching away portions of the piezoelectric layer and the lower electrode layer to expose a surface of the substrate, the portions being uncovered with the second resist film.

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15. The method of claim 14, wherein the lower electrode layer contains Pt, the piezoelectric layer contains lead titanate zirconate, and the upper electrode layer contains Au.

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16. The method of claim 14,  
wherein the substrate contains Si, and  
wherein said step of etching away the portions of the piezoelectric layer and the lower electrode layer comprises the sub-steps of:

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etching the piezoelectric layer and the lower electrode layer by first etching gas, and  
then, etching the piezoelectric layer and the lower electrode layer by second etching gas.

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17. The method of claim 16, further includes the step of:

etching the substrate so as to increase an etched portion thereof toward a surface thereof opposite to a surface thereof on which the lower electrode layer is disposed.

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18. The method of claim 17, wherein said step of etching the substrate comprises the sub-step of etching the substrate having a dummy substrate bonded thereto, with a bonding member, on the surface thereof on which the lower electrode layer is disposed.

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19. The method of claim 18, wherein the dummy substrate is made of glass, and the bonding member has a color different from a color of the substrate.

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FIG. 1

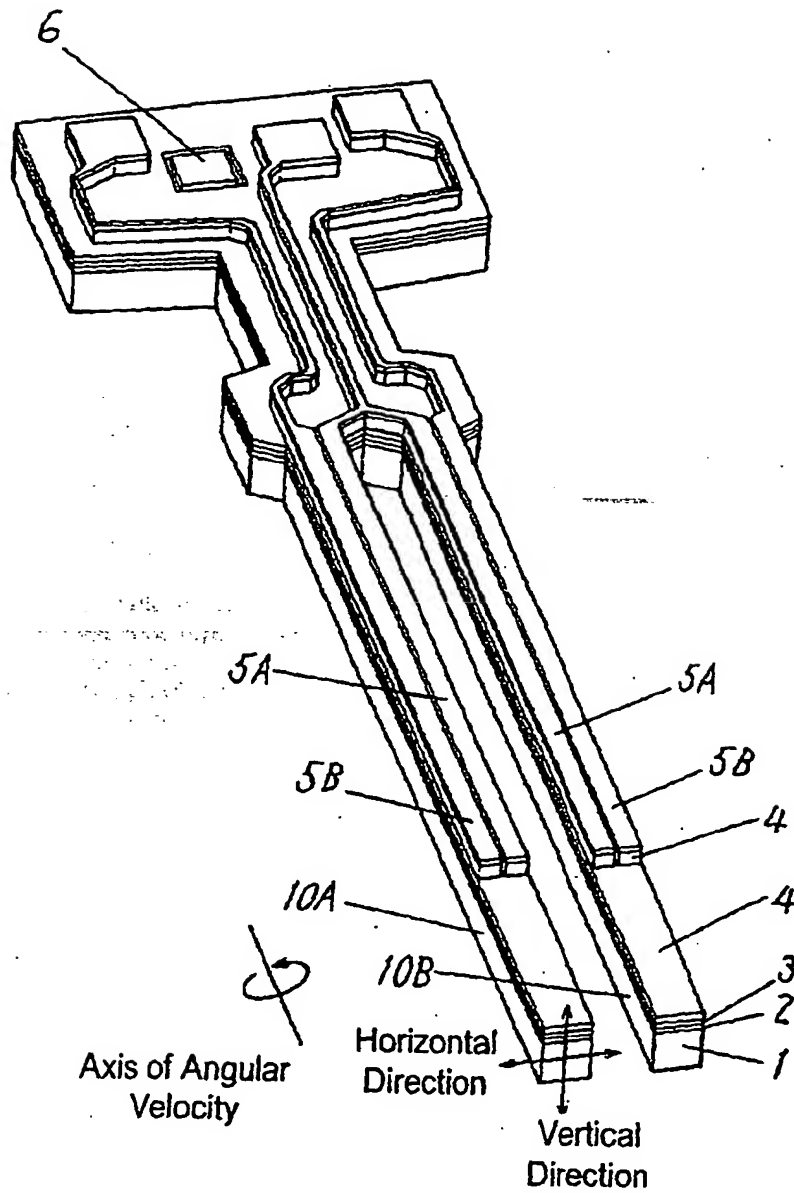


FIG. 2

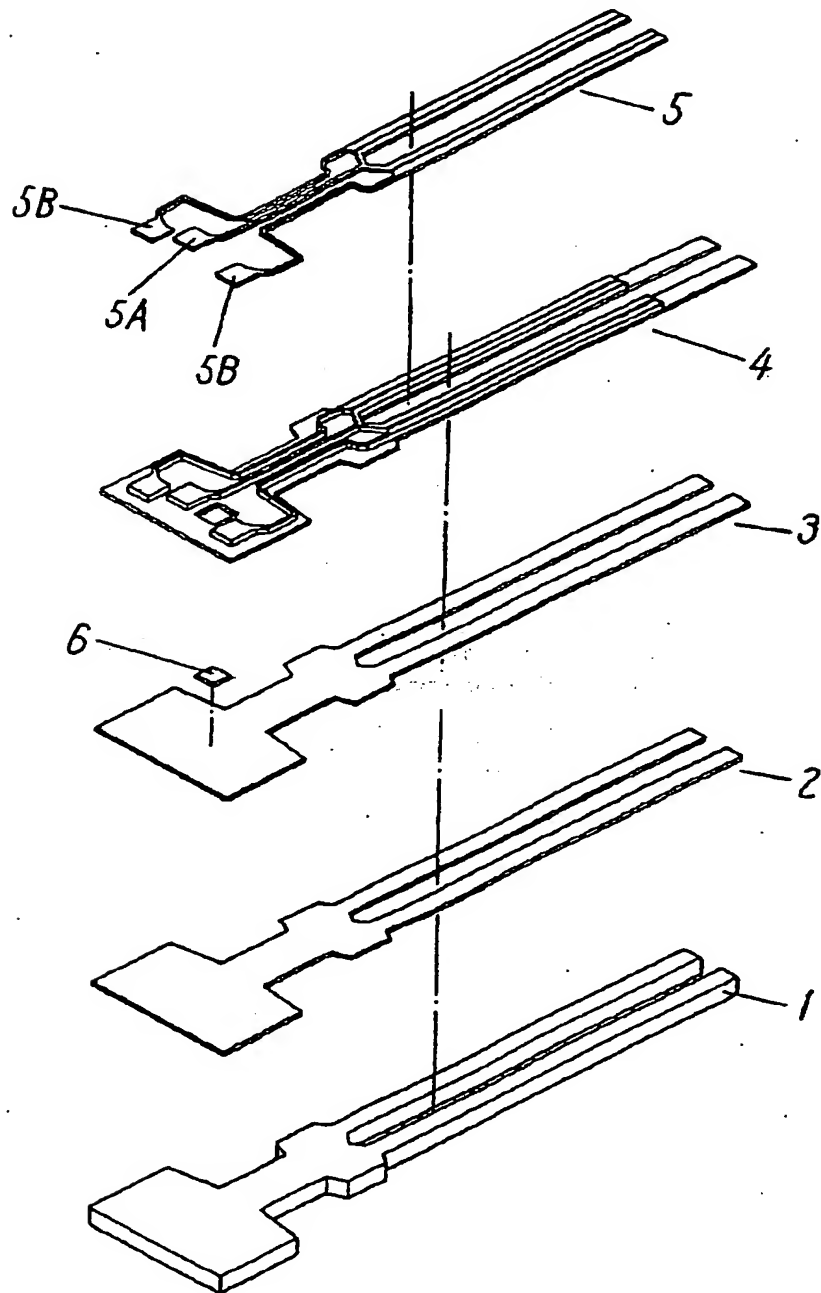




FIG. 3

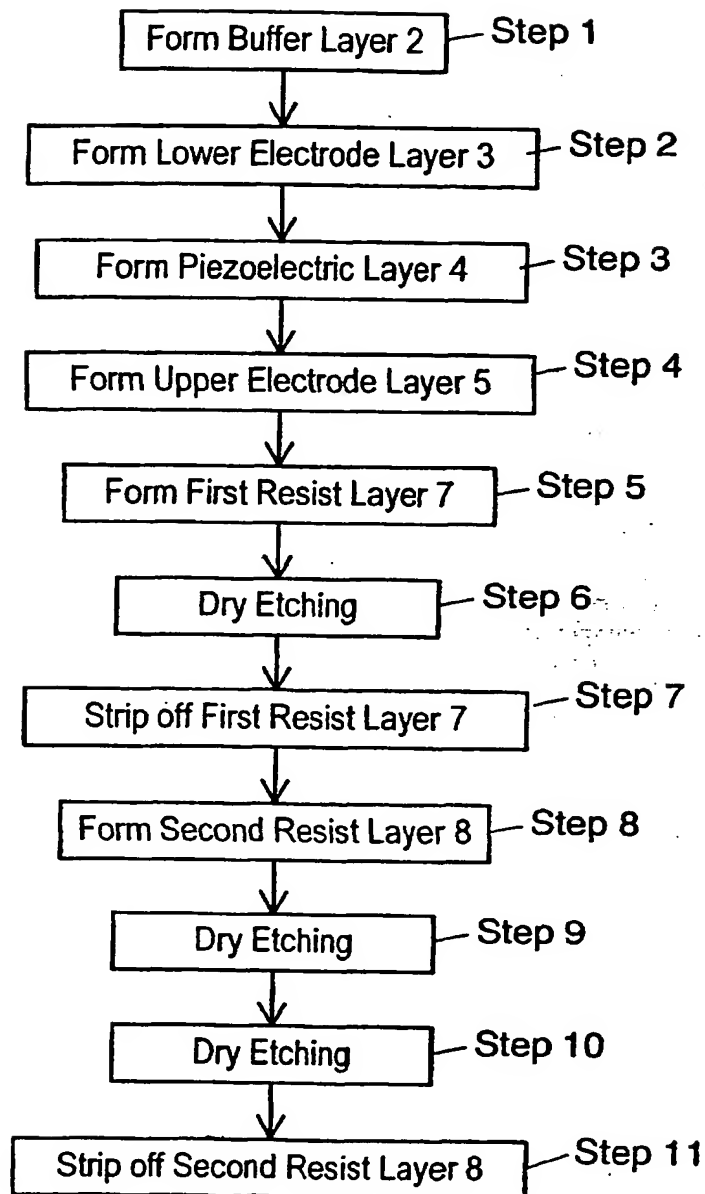


FIG. 4

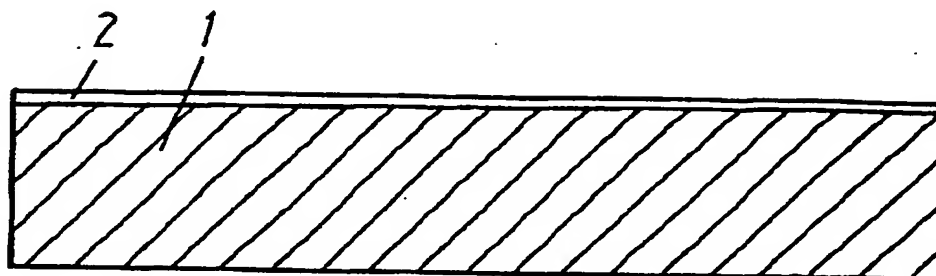


FIG. 5

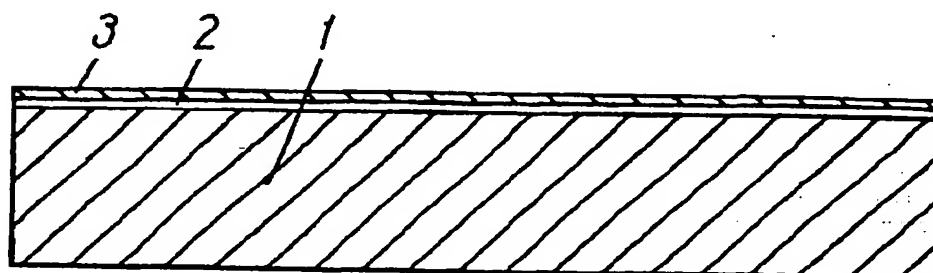


FIG. 6

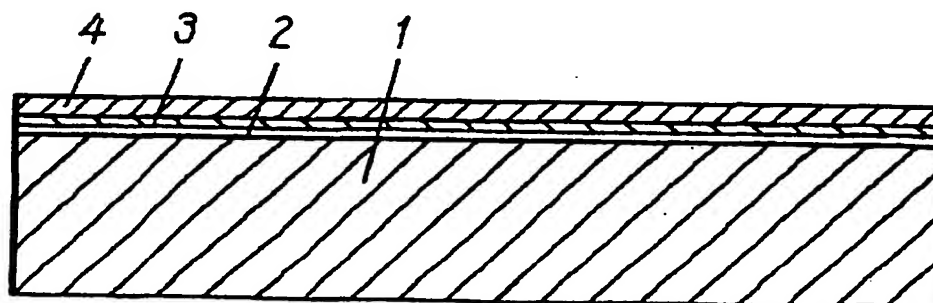


FIG. 7

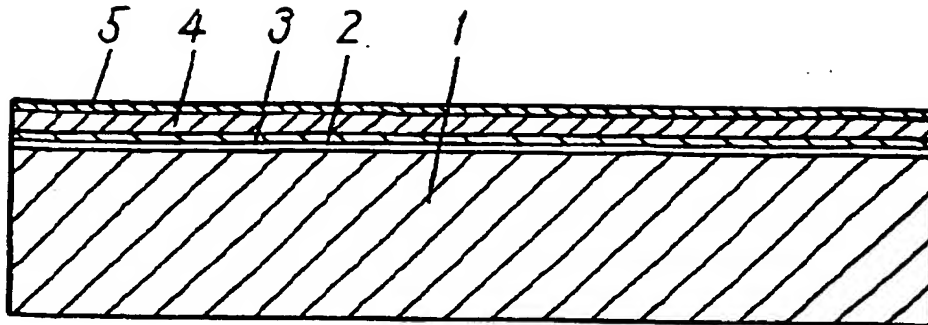


FIG. 8

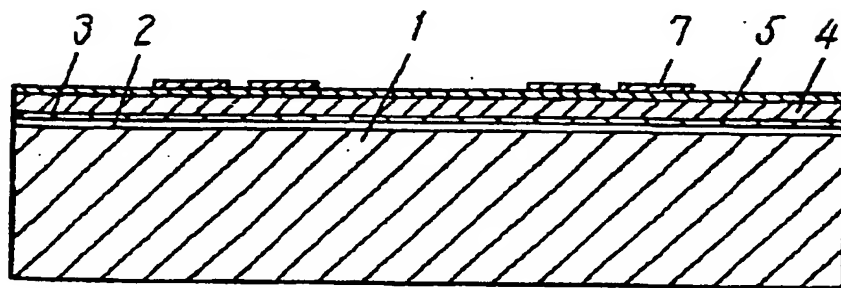


FIG. 9

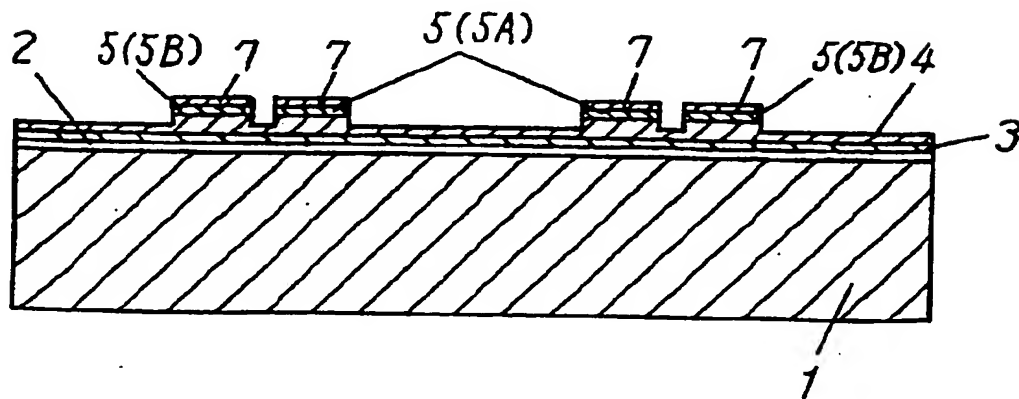


FIG. 10

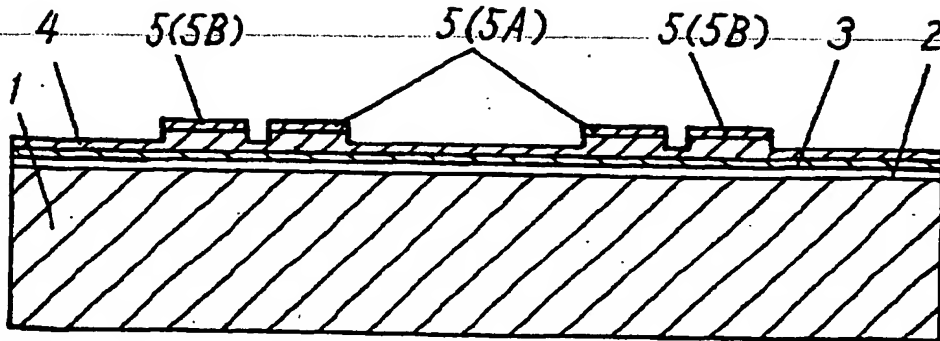


FIG. 11

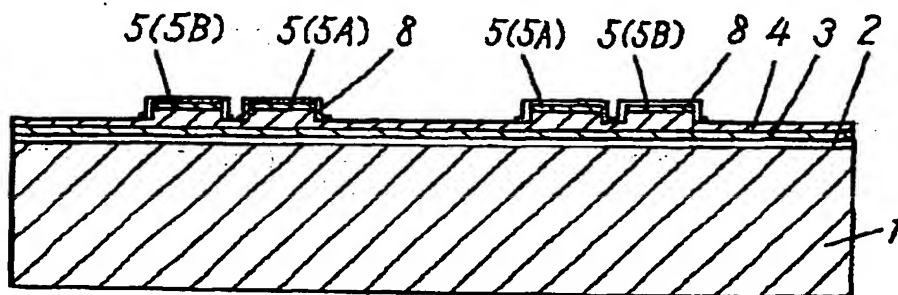


FIG. 12

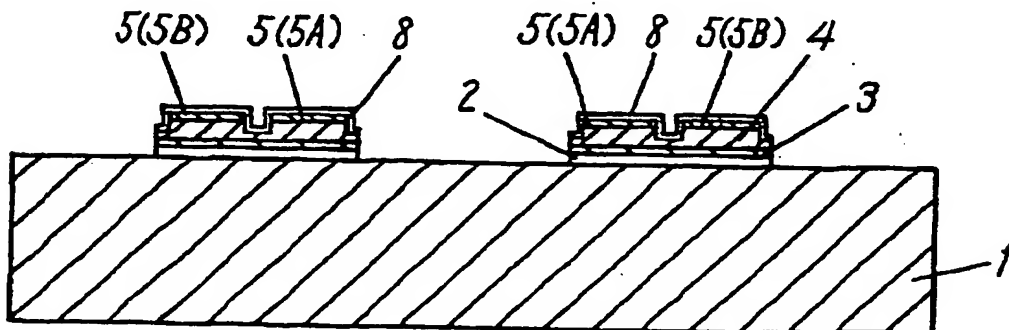


FIG. 13

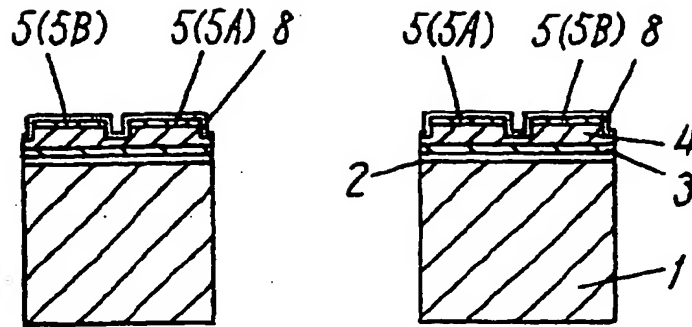


FIG. 14

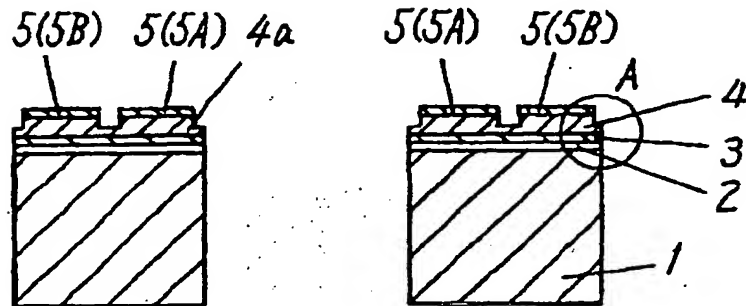


FIG. 15

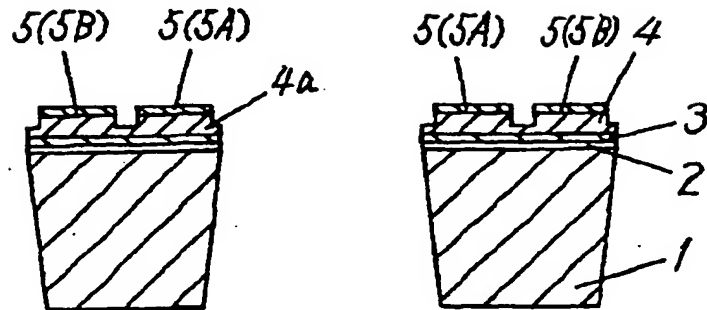


FIG. 16

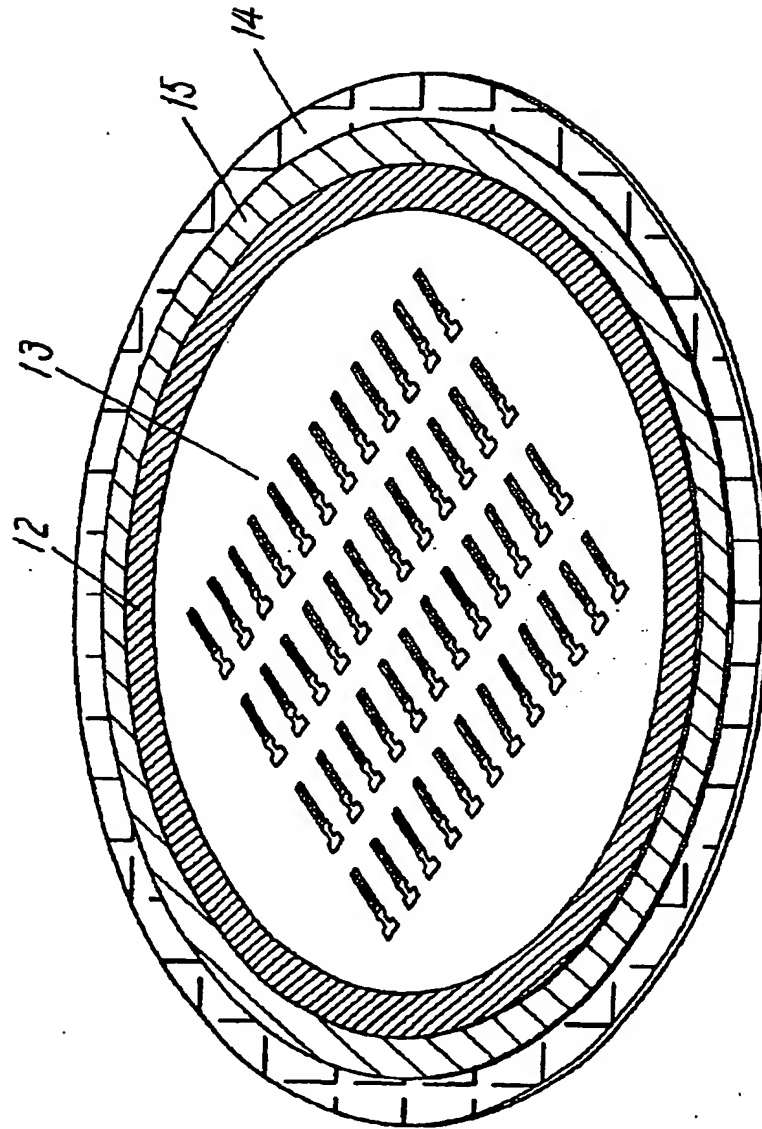
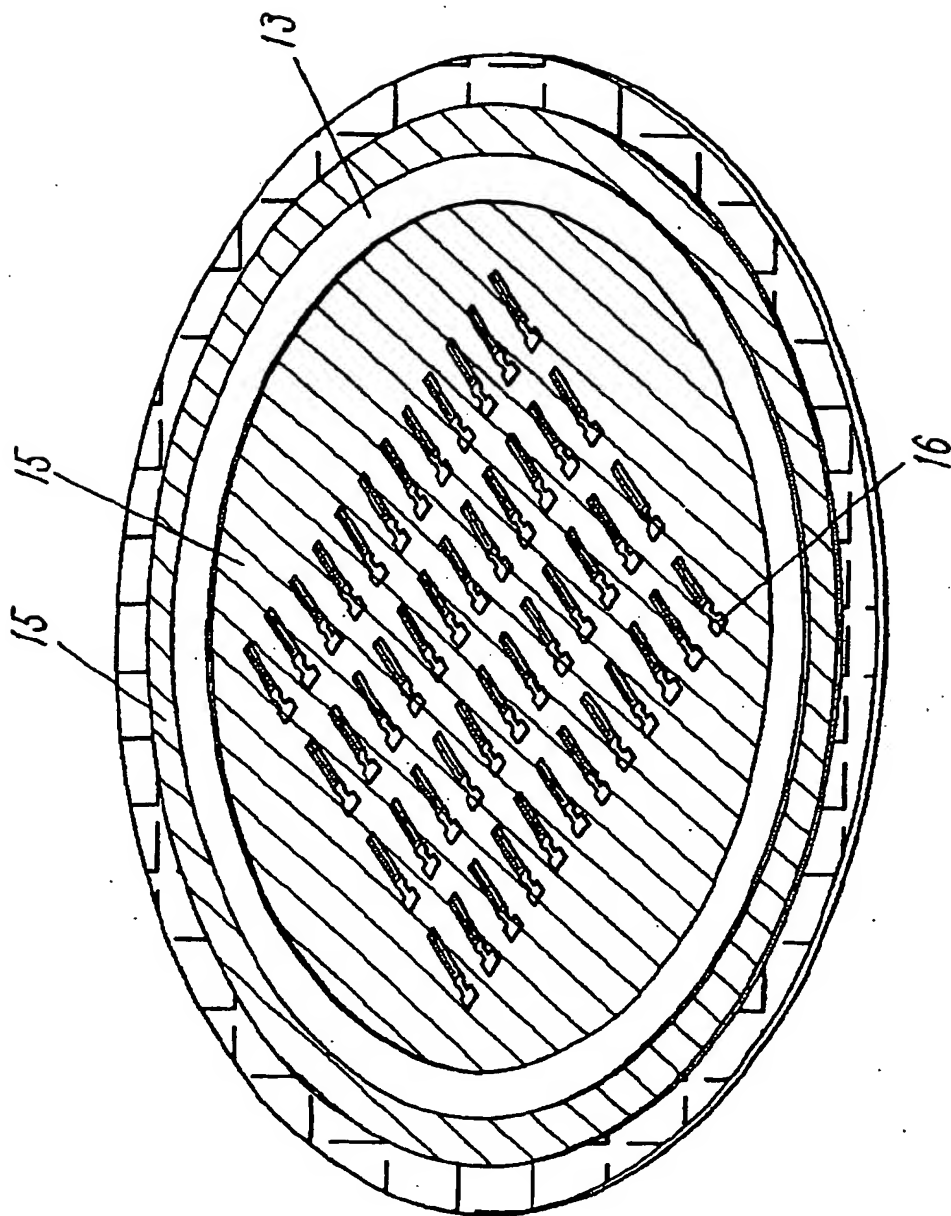


FIG. 17



**Reference Numerals**

<b>1</b>	<b>Substrate</b>
<b>2</b>	<b>Buffer Layer</b>
<b>3</b>	<b>Lower Electrode Layer</b>
<b>4</b>	<b>Piezoelectric Layer</b>
<b>4a</b>	<b>Base Portion</b>
<b>5</b>	<b>Upper Electrode Layer</b>
<b>5a</b>	<b>Exciting Electrode</b>
<b>5b</b>	<b>Detecting Electrode</b>
<b>6</b>	<b>Axially Electrode</b>
<b>7</b>	<b>First Resist Film</b>
<b>8</b>	<b>Second Resist Film</b>
<b>10A</b>	<b>Arm</b>
<b>10B</b>	<b>Arm</b>
<b>12</b>	<b>Resist Film</b>
<b>13</b>	<b>Silicon Substrate</b>
<b>14</b>	<b>Dummy Substrate</b>
<b>15</b>	<b>Bonding Member</b>
<b>16</b>	<b>Angular Velocity Sensor</b>



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP02/08056

## A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl<sup>7</sup> H01L41/09, 41/24, G01P9/04, G01C19/56

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl<sup>7</sup> H01L41/09, 41/24, G01P9/04, G01C19/56

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2002  
 Kokai Jitsuyo Shinan Koho 1971-2002 Toroku Jitsuyo Shinan Koho 1994-2002

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

JOIS

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2001-88301 A (Seiko Epson Corp.), 03 April, 2001 (03.04.01), Full text; Fig. 3 (Family: none)	1, 3 2, 4-7 8-19
X Y A	JP 6-347471 A (Canon Inc.), 22 December, 1994 (22.12.94), Full text (Family: none)	1, 3 2, 4-7 8-19
Y	US 6010919 A (Nippon Soken, Inc.), 04 January, 2000 (04.01.00), Full text; Figs. 1 to 4 & JP 9-330892 A Full text; Figs. 1 to 4 & DE 19715194 A	2

☒ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search  
07 November, 2002 (07.11.02)Date of mailing of the international search report  
19 November, 2002 (19.11.02)Name and mailing address of the ISA/  
Japanese Patent Office

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Facsimile No.

Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP02/08056

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2001-223404 A (Seiko Epson Corp.), 17 August, 2001 (17.08.01), Par. Nos. [0016] to [0018] (Family: none)	3, 4
Y	EP 675355 A (NGK Insulators, Ltd.), 04 October, 1995 (04.10.95), Columns 7, 8 & US 5698931 A & US 5825119 A & JP 7-301594 A Par. Nos. [0014] to [0015]	4, 6

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